

FOUR WAYS TO REDUCE VOIDS IN BGA/CSP PACKAGE TO SUBSTRATE CONNECTIONS

Michael A. Previti
Cookson Electronics
Johns Creek, GA, USA
mpreviti@cooksonelectronics.com

Mitch Holtzer
Cookson Electronics
South Plainfield, NJ, USA
mholzer@cooksonelectronics.com

Tom Hunsinger
Cookson Electronics
Singapore
thunsinger@cooksonelectronics.com

ABSTRACT

Voids in BGA/CSP package to substrate connections can cause issues with thermal management, drop shock resistance, and signal interference. Zero voids are always the best solution, but this is not always easy to achieve. Solder paste printing, reflow, alloy and flux chemistry all have significant influences on the amount of voiding one can expect in an assembly. This paper will discuss how print volume (stencil design), peak reflow temperature, paste flux chemistry and alloy selection affect the level of voiding to be expected when BGA/CSP packages are assembled in a lead free process.

INTRODUCTION

Voids in solder joints are considered one of the more detrimental defects in electronic assembly as area array devices have now evolved to a point where mass production of fine pitch devices with increasing functionality are common. The factors affecting void formation are complex and involve the interaction of many factors. In area array components such as BGA (Ball Grid Array), PBGA (Plastic Ball Grid Array) or CSP (Chip Scale Packages), solder joint reliability between the component and the board is one of the most critical factors as finer pitches and smaller component solder sphere volumes reduce the amount of solder in the corresponding solder joint. Voids have shown to reduce mechanical robustness of the board level interconnection and consequently affect the reliability and the conducting performance of the solder joint. The effect of voids on the reliability of a solder joint depends on size, frequency and location [1].

Voids are defined as cavities formed in the solder joint. Voids are largely caused by the amount of outgassing flux that gets entrapped in the solder during reflow [2]. Voids are essentially gas bubbles that have a much lower density

than molten solder. The buoyancy of these regions causes the bubbles to rise to the top of the solder joint [3]. Other sources of voids can be via in pad.

The outgassing flux is typically produced by the evaporation and thermal decomposition of flux constituents getting trapped in a solder joint during reflow. Reactions of chemical constituents in the flux and substrate at elevated or solder reflow temperatures are also a common cause for gas evolution. Flux is typically a complicated homogeneous solvent based mixture with many organic additives. Being organic in nature the boiling points and/or thermal decomposition temperatures of many constituents are less than 250°C. Other outgassing sources may be substances generated from or reactions with the substrate, component metalization, or the solder powder or sphere surfaces.

The location and the size of the voids are perhaps the key factors that influence the effect of the voids on the performance and reliability of solder joints. It has been an industry observation that voids in solder joints tend to accumulate towards the top of the solder joint (the interface between the package and the solder joint).

Size is perhaps the most critical factor negatively impacting the solder joint by becoming a source of entrapment, a stress riser, thermal barrier and electrical degradation by restricting the path of current flow. Larger voids typically reduce the robustness of the solder joint compared to small voids because the incidence of failure increases dramatically as the solder material thickness between the void and the ball exterior decreases. For example a 0.007" ball with a 50% void has approximately 0.0017" on each side of the void, while a 0.004" ball with a 50% void has only 0.001" on each side. The voids impact becomes more severe if it is near one of the bonding interfaces. Void location may be

equally important as reduced cross sectional area near the bonding interfaces can adversely affect reliability. A reduction in cross sectional area, specifically when voids are located at the ball/interface attach site, current flow is restricted, shear strength is reduced proportionally to the decrease in bonded material and the solder joint stability will degrade more rapidly with increased temperature cycling. Voids near the interfaces with the greatest CTE (Coefficient of Thermal Expansion) will degrade and fail in the shortest time.

A solder joint in an electronic assembly serves electrical, mechanical and thermal functions, the most important being the conduction of electrical signals. Inherently, the resistance of the solder joint should be as low as possible and there should not be much deviation in resistance between adjacent solder joints in order to achieve uniform conductivity. It has been observed in industry that the resistance of the solder joint will increase with the occurrence of large or many voids as the cross sectional area of the solder joint is considerably reduced. The mechanical function of the solder joint is to provide the connection and support to the component. The electronic component is continuously affected by the stress and strain as a result of the mismatch in the CTE, and the solder joint should be able to withstand all the stress and strain imposed on the component.

An active component in use can produce a significant amount of heat during its operation, and this heat needs to be dissipated to prevent overheating or cause the breakdown of the component. The conductive heat transfer through a solder joint can be modeled based on Fourier's law:

$$Q = KA (T1-T2)/L$$

Where Q is the heat transferred, K is the thermal conductivity, A is the cross sectional area of the solder joint, L is the length of the solid element and T1 and T2 are the temperature of the source and sink. It can be inferred from Fourier's law that the heat transferred is directly proportional to the cross sectional area. A solder joint with voids may have a greater diameter or an increased standoff to maintain the same volume in the solder joint. However, the area of cross section may or may not be the same. A solder joint with voids may have a smaller area, which may interrupt the flow of heat. No significant reliability difference has been seen with a solder joint containing no voids or small voids. However the frequency and location of the voids in a solder joint have an effect on reliability, reducing solder joint life in thermal cycle testing. Voids which are greater than 50% of the solder joint cause a potential reliability problem causing a 25-50% reduction in solder joint life in mechanical testing [1].

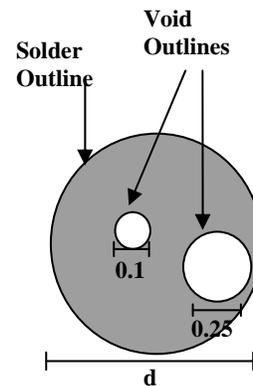
Voids themselves may not be the root cause of failures in solder joints, but voids may provide nucleation sites for defects that lead to catastrophic failure.

VOIDING

IPC-7095A is the IPC Specification for the Design and Assembly Process Implementation for BGA's. The IPC criteria provide three classes of acceptance criteria for both the solder sphere and the sphere-pad interface. Where multiple voids exist, the dimensions will be added to calculate total voiding in the joint. Inspection criteria used in this paper is the IPC 7095 requirement for solder joint area. Class III voids or better are the most desirable, being voids less than nine percent of the solder area.

Location of Void	Class I	Class II	Class III
Void in Solder (Solder Sphere)	60% of Diameter = 36% of Area	45% of Diameter = 20.25% of Area	30% of Diameter = 9% of Area
Void at Interface of Solder Sphere and Substrate	50% of Diameter = 25% of Area	35% of Diameter = 12.25% of Area	20% of Diameter = 4% of Area

Table 1: IPC 7095 Requirements for Void Classification



Example:
Total Void Diameter
 $0.10d + 0.25d = 0.35d$

Picture 1: Solder Outline with Voids

ASSEMBLY

A test vehicle was assembled to focus on issues in producing CSP/BGA in a high volume manufacturing environment. The test board used in this experiment was an existing test board designed for evaluating solder paste for processing, assembly and reliability. The test board is a 5.25 x 10.0 in., 4 layer FR-4 board. Solder mask was PSR 4000 from Taiyo. The pad finish used was Entek Plus HT copper OSP (Organic Solder Preservative) by Enthone. The component evaluated in this study attached to the test boards were 256 IO PBGA packages with lead free spheres. These PBGA packages are (17 x 17)mm, 16 x 16 full array with 1mm pitch and 0.51mm/20mil diameter solder spheres. These are supplied in SAC105 and SAC305 alloys. SACX Plus™ 0307 used in this test were re-balled onto the package. The solder paste used was a high volume commercially available paste made with SACX Plus™ 0307, SAC105 and SAC305 type 4 powder. Reflow profiles run in Figures 1 and 2 were on a Speedline Omniflo 7. All voiding X-Ray measurements were taken using a Phoenix Micromex-HLN.

Pad metallization and reflow atmosphere were not studied in this experiment as previous studies shown that these two factors do not have a significant effect on void formation [1].

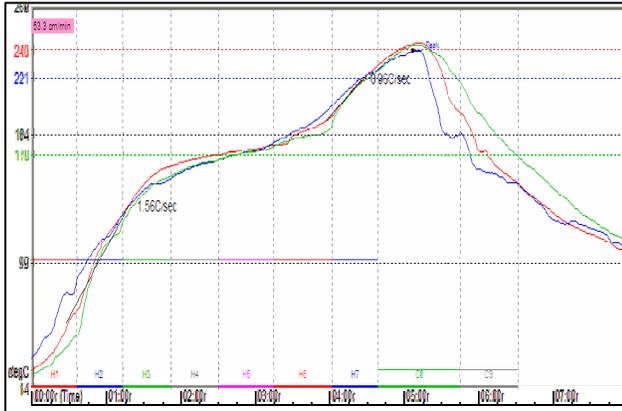


Figure 1: Low Peak Temperature, Short Soak Profile

Figure 1 shows the Low Soak profile with a 175°C soak for 60 seconds followed by a peak temperature of 240°C with total time above liquidus (TAL) of 60 seconds. The high soak profile in Figure 2 is a 160-180°C soak for 120 seconds followed by a 250°C peak temperature with a TAL of 60 seconds.

PRINTING VOLUME & STENCIL DESIGN

The goal of the solder paste printing process either on rigid or flexible circuits is simple to understand; place the correct amount of solder paste in the correct location at an acceptable rate, twenty four hours per day seven days per week. This goal may be simple to understand but the execution of the goal requires the identification, understanding, and optimization of numerous factors that all influence how well the solder paste printing process will perform.

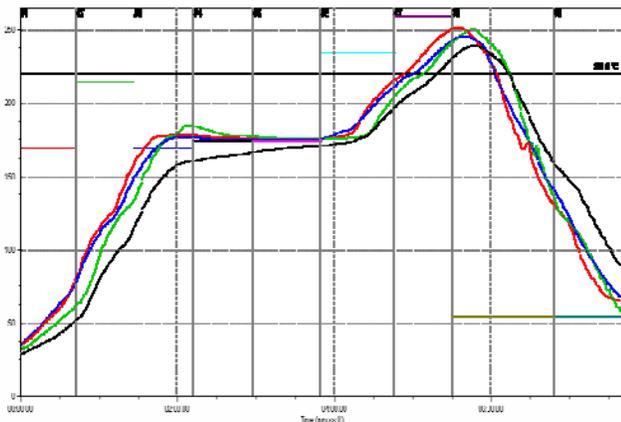


Figure 2: High Peak Temperature, Long Soak Profile

Four main elements define the typical stencil design: material, thickness, image pattern and aperture size. There is no single combination of these elements that can be recommended as the best choice. Instead, the various

options available must be considered in the context of the overall assembly process.

One of the key elements in stencil design is to maximize the amount of solder paste that is transferred through the stencil aperture onto the printed circuit board pad. This is called “transfer efficiency”. The proper stencil design will ensure the force that adheres the solder paste to the PCB pad will overcome the force that retains the solder paste in the stencil aperture. The two calculations that must be considered in stencil aperture design to maximize solder paste transfer efficiency are “aspect ratio” and “area ratio”. Aspect ratio considers the ratio between the width of the aperture and the thickness of the stencil. Area ratio considers the ratio between the opening of the aperture (the area of the printed circuit board pad that will be covered with solder paste) and the total surface area of the aperture walls. For small components where the opening of the stencil is approaching or equal to the area of the walls of the aperture, area ratio is a vital calculation to design a stencil that will print well with minimum aperture clogging and maximum solder paste transfer efficiency [4].

An aspect ratio of 1.5 or greater and an area ratio of 0.6 or greater are required to insure maximum solder paste transfer efficiency and minimum aperture clogging.

The main factors that affect solder paste printing are its rheology, tackiness, and powder particle size and shape. For example, Type 4 solder paste is typically required for pitches under 0.4mm. This is based on experimentation that has shown that four or more solder particles are needed to span the stencil aperture to achieve consistently good solder paste deposition. Similarly, with 0.3 to 0.4mm pitch, the stencil openings should be between 0.005” and 0.008” wide.

Pitch	Pad Size	Aperture	Stencil Thickness	Aspect Ratio	
Inches	µm	Inches	µm		
0.025	635	0.015 381	0.0012 305	0.006 152	2
0.020	508	0.012 305	0.010 254	0.005 - 127- 0.006 152	1.7
0.015	406	0.010 254	0.008 203	0.005 127	1.6
0.012	305	0.008 203	0.006 152	0.004 102	1.5

Table 2: Recommended sizes, pad width and tolerance

Since Type 4 paste has solder particles <0.0014”, this criterion is statistically met. Recommended paste types, based on lead pitch, are provided in Table 3.

Lead Pitch	Powder Type	Powder Size Distribution
Inches	µm	
0.025	635	3 25-45µ
0.020	508	3 25-45µ
0.016	406	3,4 25-45µ, 20-38µ
0.012	305	4 20-38µ

Table 3: Paste Type Based on Lead Pitch

Paste selection and processing parameters have been observed as critical factors affecting void formation and subsequent solder joint reliability. Figures 3 & 4 show the effect of a ten percent aperture reduction resulting in reduced volume of solder paste transferred to the corresponding pad and its affect on voiding performance. The ten percent volume reduction resulted in much lower voiding results in all cases using the same solder paste and three reflow profiles. Thus stencil design and printing parameters are critical factors in reducing voids. Figure 4 shows that size and level of voids are lowered significantly by reducing solder paste volume by approximately ten percent compared to Figure 3. under identical reflow profiles. Solder paste reduction is not seen as a drastic measure to reduce voiding as the largest volume of the solder for the joint comes from the sphere of the package being attached. However, a typical solder paste is 50% by volume flux, so the 10% reduction in solder paste volume has a larger affect on total flux content used in forming the metallurgical joint.

FLUX COMPOSITION

It is empirically observed that for the same reflow profile, different flux formulations have different voiding performance. For an identical flux formulation, different reflow profiles will yield different voiding performance. In almost all cases, a lower peak temperature profile will yield better voiding results than a higher peak temperature profile [5]. This is generally accepted as the boiling points and reaction temperature of a fluxes constituents will be further from their boiling points and reaction temperature in a lower peak temperature reflow process compared to a reflow profile having a higher peak temperature.

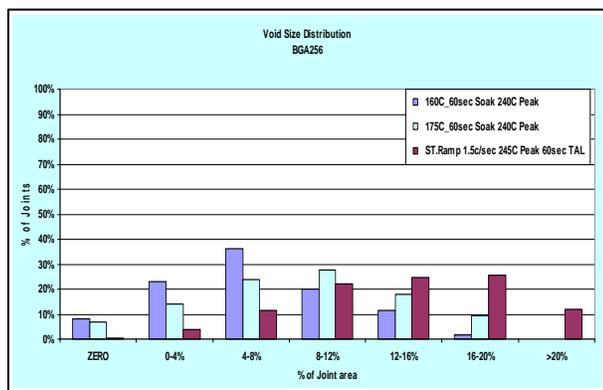


Figure 3: Void Size Distribution of BGA 256 with Three Different Reflow Profiles.

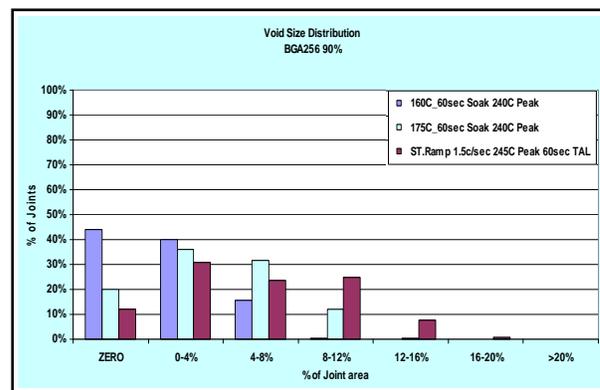


Figure 4: Void Size Distribution of BGA 256 with 10% Aperture Reduction

Another technique in flux composition evaluation is to evaluate specific components of a flux system separately and examine their direct effect on voiding based on various concentration levels. In these tests the voiding data is compared to alternative substances that may be used and run under identical conditions. Figure 5. shows an example of the difference between two different activator levels in respect to voiding keeping the reflow temperature at a 240°C peak. This provides clear evidence that different activator systems need to be evaluated when considering voiding as one material clearly shows less voiding than an alternative material. Figure 6. shows the voiding levels measured of the same flux composition run at two different reflow peak temperatures of (230 and 240) degrees Celsius. Figure 6 provides evidence that peak reflow temperature has an effect on voiding and that selecting materials with specific sublimation and boiling characteristics should be kept in mind.

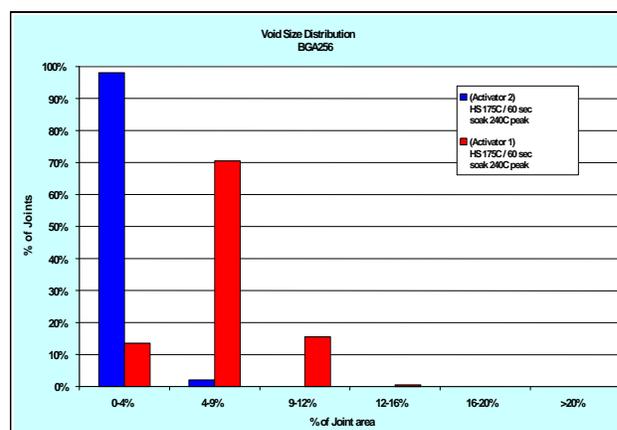


Figure 5: – Two Different Flux Activators Run at Same Reflow Temperature

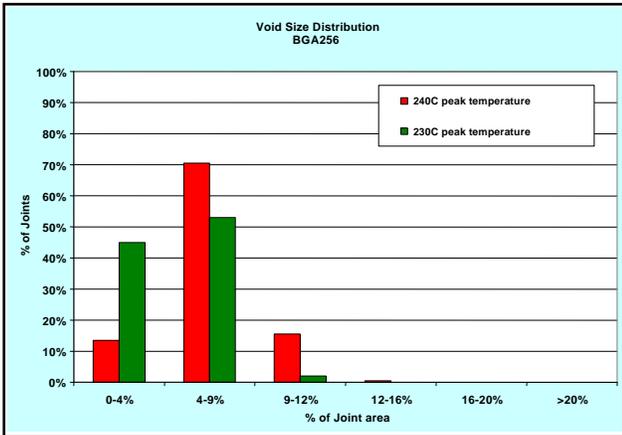


Figure 6: Voiding of same activator run at two different temperatures

Figure 7 shows the behavior of a specific constituent (Activator 1) in a DSC (Differential Scanning Calorimeter). Using a DSC measuring a single substance on a specific substrate, the reaction temperatures, boiling points and any subsequent weight loss at a specific temperature can be measured to evaluate potential voiding of a flux's constituents. This information can then be used to determine if the flux activator would be a source of voiding in a final solder paste formula. Employing the same methodology using a flux's complete activator system can also be employed. This compensates for assumptions based on boiling point depression of mixtures or unintentional reactions of these complicated systems.

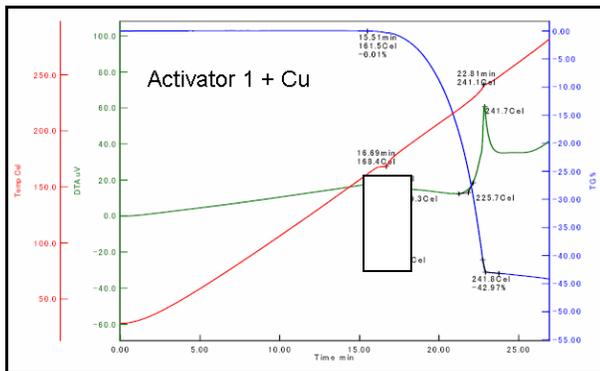


Figure 7: DSC Scan of a Solder Paste Activator Run Directly on a Copper Substrate

REFLOW PROFILE

The critical reflow profile parameters that are responsible for voiding are preheat temperature, ramp-up rate and peak temperature.

During this study all were varied within the allowable process limits to verify if voiding could be minimized. Reflow profiling and controlling ramp rate and peak reflow temperature are generally accepted as known methods of managing voiding in SMT and semiconductor package assemblies. The need for proper setup of the oven profile to limit temperature extremes and thermal shock to

components and PCB is also known. Unfortunately this is the limit of process control in many reflow processes. Many electronic assemblers ignore the potential for variance in solder joint quality due to variations in the reflow profile. Additionally, many manufacturers desire to achieve higher production volumes without increasing floor space may develop profiles that increase reflow oven belt speed to increase throughput [6]. This leads to a reduction or elimination of the soak portion of the reflow profile.

During the reflow process, the solder paste will experience temperature gradients which will impact its chemistry, voiding and the final soldering results. Proper optimization of the thermal profile will result in a net reduction of defects and increased reliability of the solder joint. In the initial ramp up stage of the profile, the low boiling solvents in the flux system will volatilize. The recommended ramp up temperature for lead free SAC reflow profiles is 0.75 - 4 degrees Celsius per second and may be limited by the thermal stability of the components. Excessive ramp up temperature may at times cause explosive release of the low boiling constituents and cause solder balls or flux spattering to appear.

The soak zone may be the most critical part of the reflow profile in which to reduce voids and subsequently the greatest area where defects have their origin. If a soak temperature is excessive, the flux constituents may be depleted. The end result will be re-oxidation of the solderable surfaces, solder powder, spheres and result in defects such as Head-In-Pillow, voiding, and improper coalescence. If the soak temperature is too low the flux may not be consumed or activated resulting in excess residues or improper solder wetting as de-oxidation has not taken place. Typical soak temperatures are usually (160 to 180)°C.

Time above liquidus (TAL) of the alloy also has an affect on solder joint reliability and defects. For SAC alloys it is recommended that a board spend approximately 60 seconds above liquidus with a peak temperature 15-20 degrees Celsius above its melting temperature. As an example, if SAC305 is used its melting temperature range is 217 to 220 degrees Celsius, the peak temperature should be in the range of 230 to 245°C. In Figure 7, the DSC exotherm demonstrates a reaction between the flux constituent and copper substrate at 247 degrees Celsius confirming at excess high temperatures other gases can be formed increasing voiding, thus excessive reflow temperatures should be avoided when targeting voiding performance.

In this study particular attention was focused on peak temperature and its affect on voiding. Besides volatilization of organic flux constituents at elevated temperatures, excessive peak temperatures can cause oxidation of the solder spheres and flux residue darkening. Excessive time above liquidus is also known to promote intermetallic growth in the solder joint causing reliability concerns. Low peak temperatures or a low amount of time above liquidus may also result in soldering defects. The issues being

typically, insufficient wetting of the solder joints or flux voids within the solder joint. The reflow profile used should remain at least 30 seconds above the liquidus temperature of the alloy.

In this experiment the data in Figure 8 came from running three solder pastes under identical reflow profiles. Solder paste A was run under both Figure 1 and 2 reflow profiles in an attempt to fine tune its optimum voiding reflow profile. In Figure 8, it can be seen that solder paste A yielded better voiding results over the other two products. This shows a solder pastes total flux system can be tuned to reduce voiding as well as the profile used affects voiding performance. Based on this study and field validation a reflow profile with a longer soak and lower peak resulted in a lower voiding system everything else being equal. This also combined with the previous flux data having higher boiling points or reaction point constituents combines in a system to reduce overall voiding effects [6].

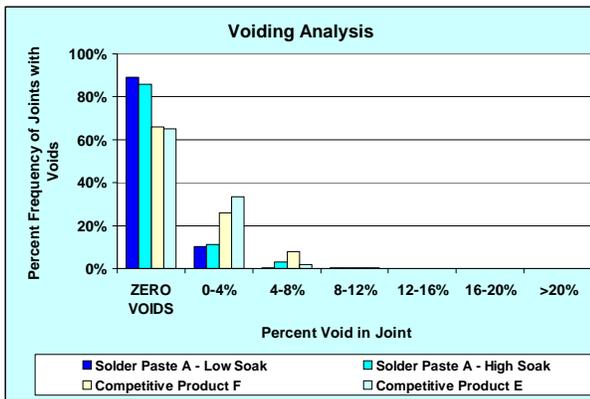


Figure 8: Voiding analyses of solder pastes in reflow profiles

ALLOY COMPOSITION

Since 2006 there has been a trend for BGA and CSP package makers to supply components with lower silver alloys. The leading low silver alloy is SAC105 with significant levels of SAC305 still being employed. SACX Plus™ 0307 & 0807 are also now being used commercially. Other alloys supplied on these packages are SAC405 and SAC387. Besides lower silver content spheres being lower cost, they are also known to have better drop shock resistance. This is typically the factor dominating their selection for hand held and consumer applications.

One of the goals of this study was to evaluate the effect of the solder sphere alloy and corresponding solder paste alloy and their total affect on voids. The study also looked at the affect of two different reflow profiles on the sphere and paste alloy matrix. Figure 9 shows the matrix of alloys studied for the sphere and solder paste. The reflow profiles used are Figures 1 and 2.

The void analyses data focused on the alloy of the sphere and paste yielded interesting results in that matching the

sphere alloy and paste alloy, resulted in most cases, in lowering voiding and void size significantly compared to mixed alloy systems. This is believed to be due to the matching melting points of the sphere and paste material during reflow. It was also observed that the high/long soak reflow profile reduced voiding in SAC105 and SAC305 combinations, but was not as pronounced with the SACX Plus™ 0307 combination.

		Sphere Alloy					
		SACX Plus™ 0307		SAC 105		SAC 305	
Paste Alloy	Reflow Profile	Short Soak	Long Soak	Short Soak	Long Soak	Short Soak	Long Soak
		SACX Plus™ 0307					
	SAC 105						
	SAC 305						

Figure 9: XY Matrix of Alloys tested and reflow profile

However the SACX Plus™ 0307 spheres in all paste alloy combinations exhibited low voiding meeting class III requirements. The SACX Plus™ 0307 alloy spheres also showed excellent voiding results with SAC105 paste, meeting Class III voiding criteria. This is believed to be due to the alloys having very similar silver and tin content. In all cases with the solder paste flux formulation which was developed with a focus on reduced voiding, class III voiding levels were attained.

In Figures 10, 11 and 12 the solid line represents the data run on the Low Soak Reflow Profile in Figure 1 with a 175°C soak of 60 seconds, a 245°C peak reflow having a TAL of 60 seconds. The dotted lines in figures 10, 11 and 12 represents the data run on the High Soak Reflow Profile Figure 2 with a 160-180°C soak of 120 seconds, a 250°C peak reflow having a TAL of 60 seconds.

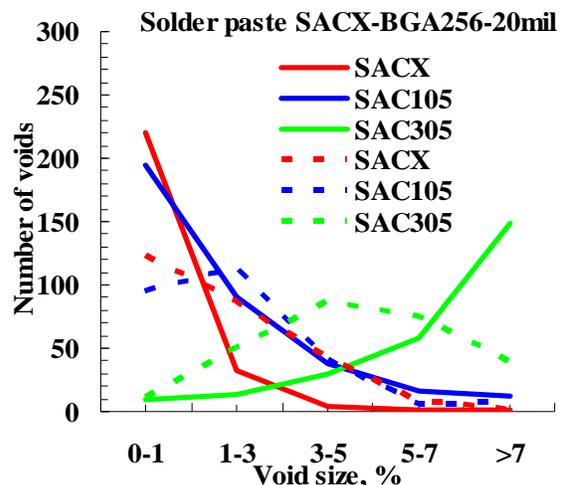


Figure 10: Voiding Analyses of SACX Plus™ 0307 Solder Paste with, SAC105 & SAC305 BGA Spheres

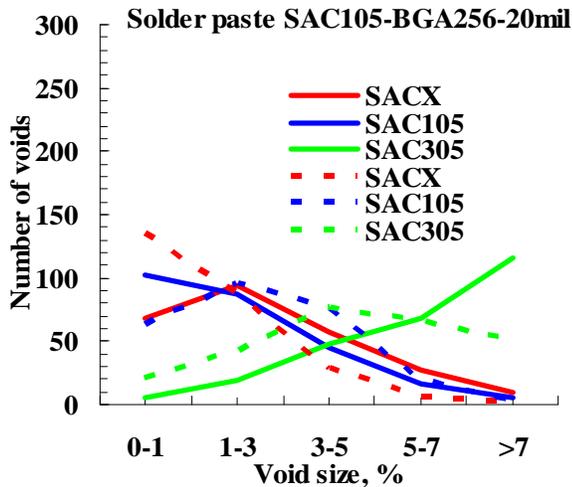


Figure 11: Voiding Analyses of SAC105 Solder Paste with SACX Plus™ 0307, SAC105 & SAC305 BGA Spheres

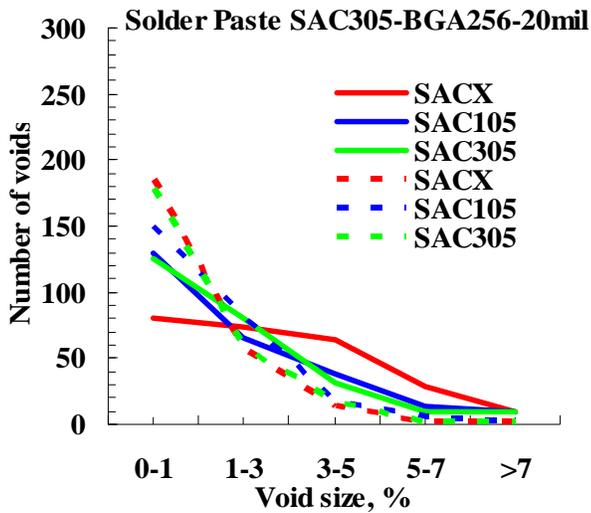


Figure 12: Voiding Analyses of SAC305 Solder Paste with SACX Plus™ 0307, SAC105 & SAC305 BGA Spheres

Figure 13 shows an X-ray photo of a SAC305 sphere BGA package with a SAC305 alloy solder paste. Voiding is minimal for this specific paste type, paste alloy and sphere alloy. Figure 14 is a similar X-Ray showing SAC305 sphere package with a SACX Plus™ 0307 solder paste. The data suggests a high silver content alloy such as SAC305 when joined with a lower silver alloy will have a higher incidence of voiding.

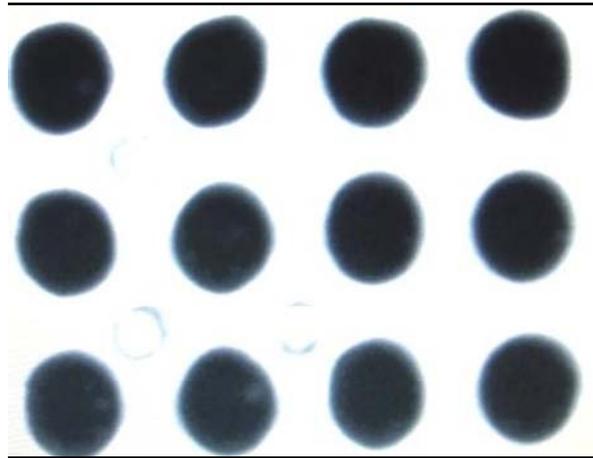


Figure 13. X-ray Image of Voids in SAC305 Sphere and Paste.

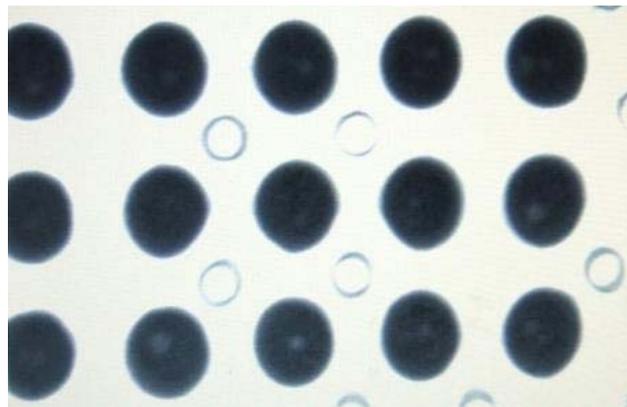


Figure 14: X-Ray Analyses SAC305 Spheres and SACX Plus™ 0307 paste

CONCLUSIONS

Combining all four aspects of alloy matching, optimized reflow while employing stencil design and a paste developed with minimizing voiding can effectively meet or exceed Class III voiding criteria.

Alloy

- Matching sphere and paste alloys tends to produce fewer large voids than mixed alloy combinations.
- The number of voids between like alloys of the solder sphere and paste were also shown to be reduced.
- SAC Plus™ 0307 spheres have overall good performance with all paste alloy combinations meeting class III voiding requirements.

Peak Reflow

- Peak reflow temperature has a significant effect on voiding due to the interaction of the flux with the copper substrate at key temperatures.
- Boards with a peak reflow of 240°C produced less voiding than the components assembled with a peak reflow of 250°C.

- The total number of voids found when comparing peak temperature of the reflow were about 25-30% higher for a peak temperature of 250°C than for a peak of 240°C.
- Boards assembled using a low ramp rate of 0.75°C/sec produced less voiding than the boards assembled using a faster ramp rate.

Flux Formulation

- Solder paste formulation has a significant effect on voiding due to the type of chemistries used and where they become reactive with the copper substrate.
- A solder paste flux system developed for low voiding can still be affected by the reflow profile, soak and peak reflow temperatures.

Solder Paste Volume

- Reduced volume of paste and/or sphere reduces voiding.
- A 10% solder paste reduction by stencil design has shown to decrease BGA voiding significantly.

ACKNOWLEDGEMENTS

The authors would like to thank the Cookson America & India Research Centers for the board assembly, flux formulation work and analyses.

REFERENCES

- [1] M. Yunis, K. Srihari, J.M. Pitarresi, A. Primavera. "Effects of voids on the reliability of BGA/CSP solder joints," *Microelectronics Reliability* 43, (2003) 2077-2006, Elsevier Ltd.
- [2] LeeNch, O'Hara, Voiding in BGA. In: *Proceeding of Surface Mount International*, San Jose, California, 1995.
- [3] Hwang JS, *Solder paste in electronics packaging*, New York; Van Nostrand Reinhold; 1989.
- [4] R. Pandher, C. Shea, *Optimizing Stencil Design for Lead-Free Processing*, *Proceeding of Surface Mount International*, Chicago, Illinois, 2004.
- [5] M. Holtzer, *BGA Voiding Prevention*, Technical Report, Cookson Electronics, South Plainfield, New Jersey, 2009.
- [6] S. Eckel, N. Kani, D. Le, "Impact of PCB Surface Pad Finish and Contamination on BGA Solder Joint Voiding", *Proceeding of Surface Mount International*, September, 2001.